IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Manjul Bhushan
Mark C. Ketchen

Docket No.: YOR920030032US1

Serial No.: Unassigned

Filing Date: Concurrently Herewith

Title: **METHOD AND APPARATUS FOR DETERMINING CHARACTERISTICS OF MOS DEVICES**

INFORMATION DISCLOSURE STATEMENT

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, Applicants' attorney wishes to bring to the attention of the Patent and Trademark Office the following document listed on the accompanying PTO Form 1449. A copy of the listed item is enclosed.
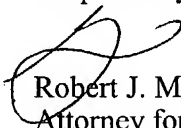
Other Documents

1. Taur et al., "Fundamentals of Modern VLSI Devices," 5.3 Sensitivity of CMOS Delay to Device Parameters, 5.3:1-4.3, pgs. 257-273 (1998).

The filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made, or as an admission that the information cited is considered to be material to patentability or that no other material information exists.

Respectfully submitted,

Date: July 18, 2003

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LIST OF PUBLICATIONS FOR
APPLICANT'S INFORMATION
DISCLOSURE STATEMENT

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NO.	DATE	NAME	CLASS/SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NO.	DATE	COUNTRY	CLASS/SUBCLASS	TRANSLATION YES NO

OTHER DOCUMENTS

EXAMINER INITIAL	REF NO.	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
		Taur et al., "Fundamentals of Modern VLSI Devices," 5.3 Sensitivity of CMOS Delay to Device Parameters, 5.3:1-4.3, pgs. 257-273 (1998).

Examiner _____   Date Considered _____

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.